



## Semi-Custom Bipolar Array Design Story

ISO9001:2000 Certified

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- What do I do when I require reduced board area?
- What if I don't have 36 weeks to get the first pass at a full custom ASIC?
- What if I can't afford the up-front costs to spin an ASIC?
- How can I get into an analog IC with my own intellectual property?
- How do I add functionality to an existing product that no longer has empty board space?
- Where do customers go who only need a few thousand pieces a year for their product, don't have a standard integrated circuit that is made for their design, and need to integrate some analog functions with a small amount of digital.

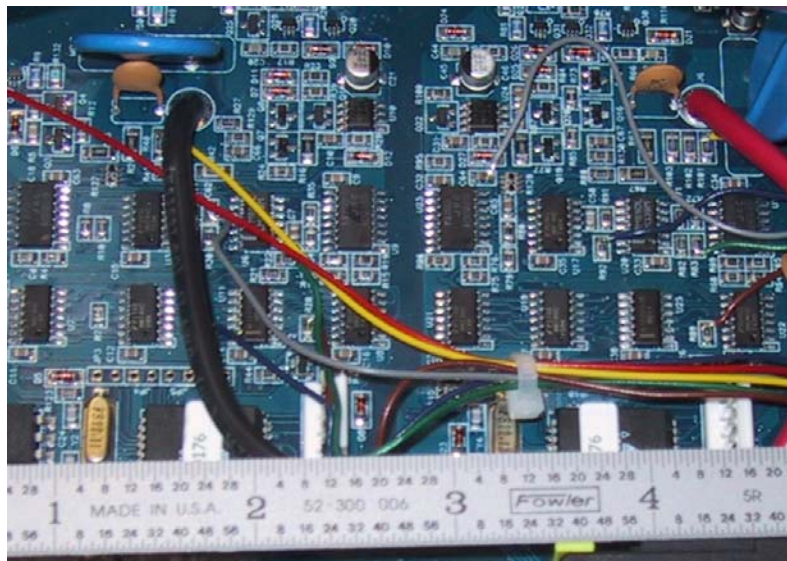
These were questions we asked ourselves when we were faced with a customer problem. Getting to market in a timely manner without spending \$500K to \$1 million is tough. Most fabs are moving towards larger wafer sizes, and a full wafer run can easily produce 100's of thousands of parts.

Using semi-custom analog allows a customer to develop an ASIC for a lower volume application. This approach also enables the fabrication of full wafer lots up to the metal mask layer, sharing mask costs and production costs. These wafers are customized per customer order within two weeks of fabrication time.

We had a customer with the above problems who approached us about getting a quick-turn analog ASIC at a lower than normal NRE. We used the Arrays and solved the customer's problem.

The original design took 8.3 square inches of board area. There were 18 ICs and around 130 discrete devices. Some functions were not included in the original design since there was not enough room on the board. These functions were added to the final product. Some of the ICs were HCMOS digital logic. The following table shows what was replaced, not including discretes.

- (4) 74HC74 HCMOS Flip Flops
- (2) 74HC14 HCMOS Schmitt Triggers
- (2) 74HC08 HCMOS AND Gates
- (2) 74HC11 Triple 3-input AND gates
- (2) LM339 Comparators
- (4) LM13700 Trans-impedance Amps
- (2) LM338 Comparators
- (2) TLC272C – Amplifiers



12 Weeks Later →



(28 SOIC)



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### ***Design Span:***

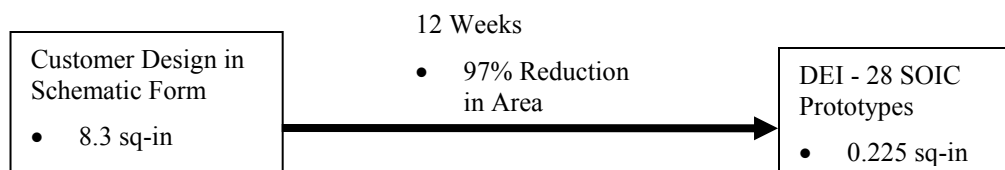
From the time the first meeting took place to the time the customer received prototypes was **12 weeks**. In this time:

- DEI met with the customer to clarify circuit specifications. Customer supplied schematic and described additional circuitry that they wanted to add.
- DEI's designer learned SIMetrix flow and investigated possible solutions. Solutions were based on published circuits in the Design Manual as well as other sources.
- We discussed circuit changes and put together initial circuit design and sent to customer. Customer reviewed circuit schematics and simulations. Customer acquired SIMetrix and performed some simulations to analyze the design.
- DEI assisted the customer to breadboard the circuit and evaluate it in their application. This was done with actual array elements packaged in 18 pin DIPs so you use Array transistors.
- Here is a list of the available elements:

Kit Part	Contents
7KP1	Six Small NPN with single emitter.
7KP2	Six Small NPNs. Two with 3 emitters, two with 2 emitters, and two with 1 emitter.
7KP3	Four small PNP with separate collectors, one epi-pinch.
7KP4	Two large NPN, two large PNP, one small NPN, and one small PNP.
7KP7	Six Schottky-clamped NPN with one emitter connected to substrate.

- We finished circuit design and verification with the breadboard over the next few weeks.
- We conducted a Critical Design Review with the customer to review final design and simulations. Customer signed off design upon completion of CDR action items.
- Netlist was sent to the designer of the arrays for layout, layout versus the schematic (LVS) checking, and Design Rules Check (DRC).
- Design was fabricated and packaged. Returned finished goods to customer in three weeks.
- The design worked the first time!

Here is a flowchart and some specifics about the design. We enabled a new commercial product for the customer by reducing the board space from 8.2 square inches to about 0.225 square inches, a 97% reduction in board area. This space reduction took what was only available in high end systems and enabled it to be put into a small box for commercial applications. This resulted in a significant reduction in cost.





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### **Design Tools:**

As you can see above, the customer used the same tools that DEI used, and this enabled them to insure that the design effort was successful. The customer did do simulations, but they did not do layout. Tools are available for customers to do both. Below is a table showing which tools are included with each package available from Device Engineering. Please contact Device Engineering for updated pricing.

Function	Tool	DEI-700-DS-SLV	DEI-700-DS-GOLD	DEI-700-DS-PL
Schematic and Sim Full	SIMetrix Micron AD	Yes	Yes	Yes
Layout	ICED	No	Yes	Yes
Design Rules Check	ICED-DRC	No	No	Yes
Layout Versus Schematic	ICED-LVS	No	No	Yes
Scripts		Yes	Yes	Yes
Sample Files		Yes	Yes	Yes
Libraries (as available)		Yes	Yes	Yes
Budgetary Price		Consult Factory	Consult Factory	Consult Factory

\* SIMetrix Micron AD Includes Noise Analysis and Monte Carlo Analysis.

SIMetrix is a SPICE based simulator with a good GUI. This simulator includes Monte-Carlo analysis which varies parameters in your design much like a fab process would. This verifies that the design is manufacturable. The tool also includes noise analysis for more in-depth circuit checkout.

ICED is an easy to use, PC based layout tool that allows a customer to do their own layout. Because there is only one layer of metal to define in the arrays, which allows most customers the chance to do their own layout, further reducing NREs. An engineer doing the layout needs only to select and place an array; place the NPNs, PNPs, and other device overlays (identify a unique block for Layout Versus Schematic Checks); and wire the device. Different colors are available for routing for identification and are combined on the same layer in the metal mask. After this is complete, LVS and DRC are run followed by the generation of a GDSII stream file. This starts the three week process to prototypes in ceramic packages.

### **Your Array Design at DEI:**

- DEI can provide test services as necessary.
- DEI stages wafers for three week prototype turn.
- DEI can do Military group testing and flows for array designs.
- DEI can provide full turnkey design services, netlist input to finished goods, or any portion of the design task.

Notes:

SIMetrix is a product of Newbury Technology (<http://www.newburytech.co.uk>).

ICED is a product of IC Editors, Inc.