

**DEVICE
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**DEI1054
Six Channel
Discrete-to-Digital Interface
Sensing 28 Volt/Open**

Features

- Small footprint (16L SOIC NB)
- Senses six 28V/Open discrete logic signals
- Inputs are Lightning Protected to DO-160D Level 3
- TTL/CMOS-Compatible Tri-state Outputs
- Package / Temperature Options:
 - 16L 150mil SOIC, -55°C/+85°C
 - 16L Ceramic 300mil SOP, -55°C/+125°C



Functional Description

The DEI1054 is a six channel discrete-to-digital interface BiCMOS device. It senses six 28V/Open discrete signals of the type commonly found in avionics systems. The inverted outputs are TTL/CMOS compatible and are enabled via the \overline{CE} and \overline{OE} pins. The input pins of this small, 16-lead narrow body SOIC device are lightning protected to meet the requirements of DO160D waveforms 3, 4, and 5, level 3. See figures 5-7.

With its reliability, low cost, operating range, and lightning protection, the DEI1054 meets a large variety of interface requirements for aerospace and industrial applications.

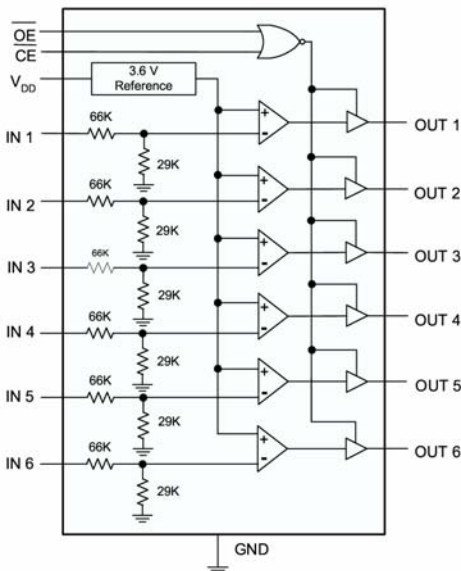


Figure 1: Function Diagram

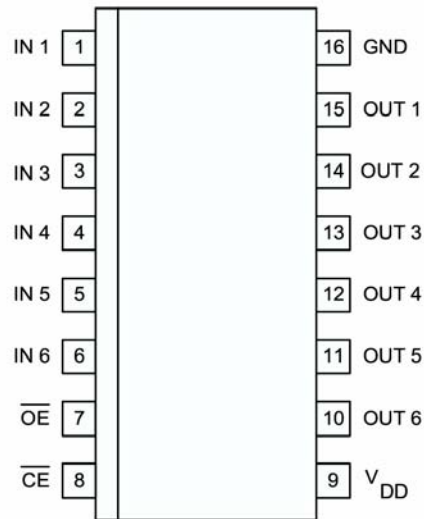


Figure 2: Pinout Diagram

Table 1: Absolute Maximum Ratings (Note 1)

PARAMETER	MIN	MAX	UNITS
Supply Voltage V_{DD}	-0.3	7.0	V
Discrete Input Voltage (Pins 1-6) Continuous (Note 2):	-80	+80	V
Lightning Protection (Pins 1-6): DO160D, Waveform 3; Level 3	-600	+600	V
DO160D, Waveforms 4 and 5; Level 3	-300	+300	V
Digital Input Voltage (\overline{CE} and \overline{OE})	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
Storage Temperature	Plastic Ceramic	145 175	°C
Junction Temperature T_{JMAX}		145	°C
Body Soldering Temperature, 10sec (JEDEC J-STD-20)	-	235	°C

The DEI1054 contains circuitry to protect inputs against damage due to high voltage static discharge. It has been characterized per JEDEC A114-A Human Body Model to Class 1. Observe precautions for handling and storing Electrostatic Sensitive Devices.

Notes:

1. Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.
2. The DEI1054 will withstand the transient surge DC voltage step function loci limits for category B equipment per MIL-STD-704A.

Table 2: DEI1054 Device Operating Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Free Air Operating Temp.	T_A	$V_{DD} = 4.5 - 5.5 V$	-55		+85	°C
Plastic Ceramic			-55		+125	
Logic Output Sink Current	I_{OL}	$V_{DD} = 4.5 - 5.5 V$			5.0	mA
Logic Output Source Current	I_{OH}	$V_{DD} = 4.5 - 5.5 V$	-5.0			mA

Table 3: DEI1054 Logic Truth Table

\overline{CE} (Chip Enable)	\overline{OE} (Output Enable)	IN 1-6 Input	OUT 1-6 Output
0	0	Open	1
0	0	28 Volts	0
1	X	X	High Z
X	1	X	High Z

Table 4a: DE11054 (Plastic) Electrical Characteristics
 (T_A = -55°C TO +85°C, V_{DD} = 4.5 TO 5.5 V, Unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply and Thermal Data						
Supply Current	I _{DD}	IN 1-6 = 0V \overline{OE} , \overline{CE} , V _{DD} = 5.5 V		5	10	mA
Thermal Resistance	θ _{JA} θ _{JC}	Junction to Ambient (4L PCB) Junction to Case		74 24		°C/W
Discrete Input Characteristics						
IN 1-6 input voltage for Open input sense	V _{SO}	Voltage source from input terminal to ground for Logic High Output.	-5		10	V
IN 1-6 input current for Open input sense	I _{SOmax}	Maximum input current to produce Logic High output.			80	µA
IN 1-6 input voltage for 28V input sense	V _{S28}	Voltage source from input terminal to ground for Logic Low Output.	14		35	V
IN 1-6 input current for 28V input sense	I _{S28min}	Minimum input current to produce Logic High output.	187			µA
IN 1-6 Input Resistance	R _{IN}	Discrete input resistance. 0V < IN 1-6 < 16V	71	95	119	KΩ
IN 1-6 Input current at 28V	I _{IN28}	V _{IN} = 28V			502	µA
Logic Input Characteristics						
\overline{CE} , \overline{OE} input logic 1 level	V _{IH}		2.0			V
\overline{CE} , \overline{OE} input logic 0 level	V _{IL}				0.8	V
DC Output Characteristics						
Output logic 1 level (TTL)	V _{OH}	I _{OH} = -5 mA.	2.4			V
Output logic 0 level (TTL)	V _{OL}	I _{OL} = 5 mA.			0.4	V
Output logic 1 level (CMOS)	V _{OH}	I _{OH} = -100 µA (Note 1)	V _{DD} - 50mV			V
Output logic 0 level (CMOS)	V _{OL}	I _{OL} = 100 µA (Note 1)			V _{SS} + 50mV	V
Off-state Output Current	I _{OZ}	OE = V _{DD} V _{DD} = 5.5 V V _{OUT} = 0 or V _{DD}			+/-10	µA
Switching Characteristics (Note 1)						
I/O propagation delay	t _{HL} , t _{LH}	Refer to Figure 4.			500	ns
Delay from \overline{CE} or \overline{OE} input (with output low) to output HI-Z	t _{LZ}	Refer to Figure 3.			25	ns
Delay from \overline{CE} or \overline{OE} input (with output HI-Z) to output low	t _{ZL}	Refer to Figure 3.			25	ns
Delay from \overline{CE} or \overline{OE} input (with output high) to output HI -Z	t _{HZ}	Refer to Figure 3.			25	ns
Delay from \overline{CE} or \overline{OE} input (with output HI-Z) to output high	t _{ZH}	Refer to Figure 3.			25	ns

NOTES:

1. This parameter is guaranteed by design and not tested.

Table 4a: DE11054 (Ceramic) Electrical Characteristics
 ($T_A = -55^\circ\text{C TO } +125^\circ\text{C}$, $V_{DD} = 4.5 \text{ TO } 5.5 \text{ V}$, Unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply and Thermal Data						
Supply Current	I_{DD}	IN 1-6 = 0V \overline{OE} , \overline{CE} , $V_{DD} = 5.5 \text{ V}$		5	10	mA
Thermal Resistance	θ_{JA} θ_{JC}	Junction to Ambient (4L PCB) Junction to Case		TBD 23		$^\circ\text{C/W}$
Discrete Input Characteristics						
IN 1-6 input voltage for Open input sense	V_{SO}	Voltage source from input terminal to ground for Logic High Output.	-5		10	V
IN 1-6 input current for Open input sense	I_{S0max}	Maximum input current to produce Logic High output.			80	μA
IN 1-6 input voltage for 28V input sense	V_{S28}	Voltage source from input terminal to ground for Logic Low Output.	14		35	V
IN 1-6 input current for 28V input sense	I_{S28min}	Minimum input current to produce Logic High output.	187			μA
IN 1-6 Input Resistance	R_{IN}	Discrete input resistance. $0\text{V} < \text{IN } 1-6 < 16\text{V}$	71	95	119	$\text{K}\Omega$
IN 1-6 Input current at 28V	I_{IN28}	$V_{IN} = 28\text{V}$			502	μA
Logic Input Characteristics						
\overline{CE} , \overline{OE} input logic 1 level	V_{IH}		2.0			V
\overline{CE} , \overline{OE} input logic 0 level	V_{IL}				0.8	V
DC Output Characteristics						
Output logic 1 level (TTL)	V_{OH}	$I_{OH} = -5 \text{ mA}$.	2.4			V
Output logic 0 level (TTL)	V_{OL}	$I_{OL} = 5 \text{ mA}$.			0.4	V
Output logic 1 level (CMOS)	V_{OH}	$I_{OH} = -100 \mu\text{A}$ (Note 1)	$V_{DD} - 50\text{mV}$			V
Output logic 0 level (CMOS)	V_{OL}	$I_{OL} = 100 \mu\text{A}$ (Note 1)			$V_{SS} + 50\text{mV}$	V
Off-state Output Current	I_{OZ}	$OE = V_{DD}$ $V_{DD} = 5.5 \text{ V}$ $V_{OUT} = 0 \text{ or } V_{DD}$			+/-10	μA
Switching Characteristics (Note 1)						
I/O propagation delay	t_{HL} , t_{LH}	Refer to Figure 4.			500	ns
Delay from \overline{CE} or \overline{OE} input (with output low) to output HI-Z	t_{LZ}	Refer to Figure 3.			30	ns
Delay from \overline{CE} or \overline{OE} input (with output HI-Z) to output low	t_{ZL}	Refer to Figure 3.			30	ns
Delay from \overline{CE} or \overline{OE} input (with output high) to output HI -Z	t_{HZ}	Refer to Figure 3.			30	ns
Delay from \overline{CE} or \overline{OE} input (with output HI-Z) to output high	t_{ZH}	Refer to Figure 3.			30	ns

NOTES:

1. This parameter is guaranteed by design and not tested.

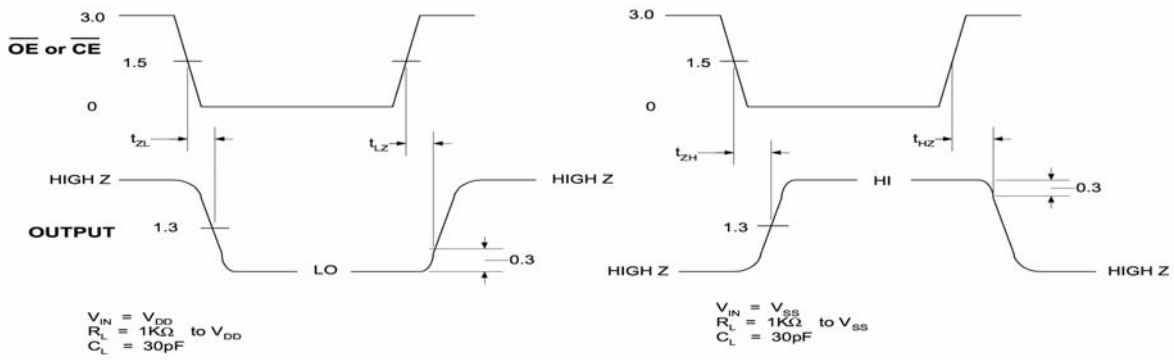


Figure 3: Enable to Output Propagation Delay

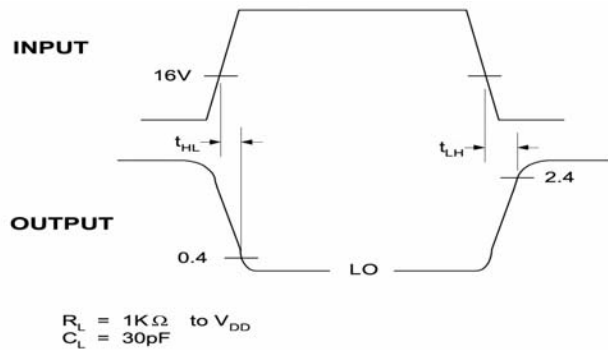


Figure 4: Input to Output Propagation Delay

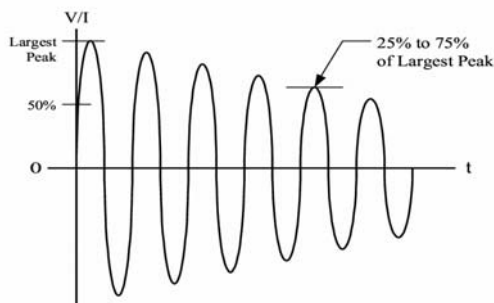


Figure 5: DO160D Voltage Waveform #3
 $V_{oc} = 600V$, $I_{sc} = 24A$, Frequency = $1.0MHz \pm 20\%$

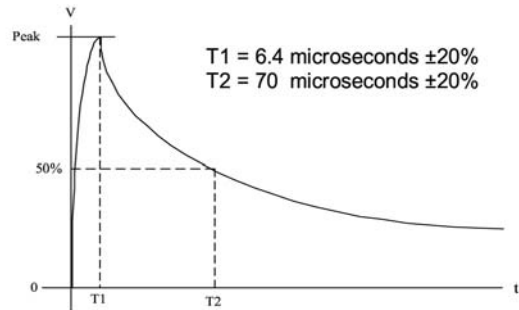


Figure 6: DO160D Voltage Waveform #4
 $V_{oc} = 300V$, $I_{sc} = 60A$

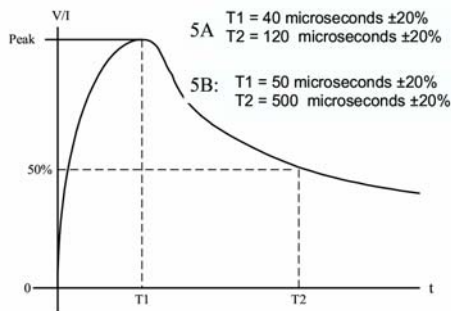
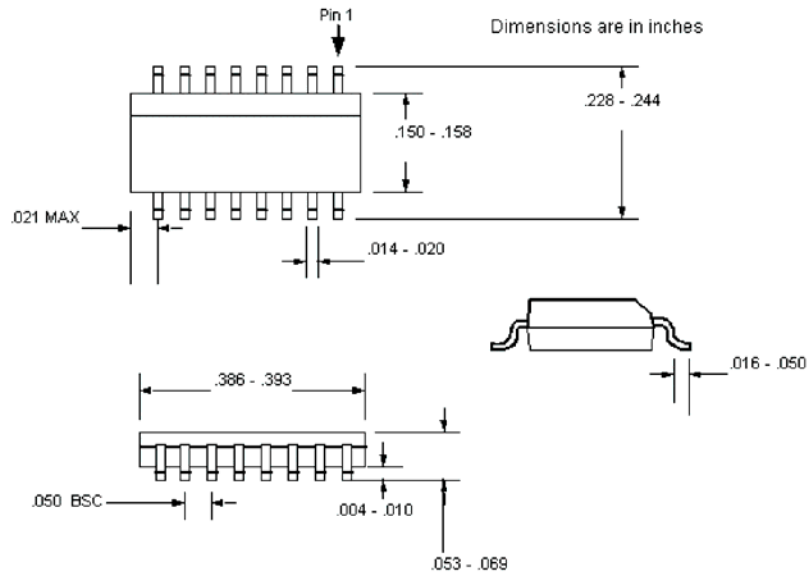


Figure 7: DO160D Voltage Waveform #5

Notes:

1. V_{oc} = Peak Open Circuit Voltage available at the calibration point.
2. I_{sc} = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%
4. The ratio of V_{oc} to I_{sc} is the generator source impedance to be used for generator calibration purposes.

Package Descriptions
16L 150mil SOIC



Moisture Sensitivity: JEDEC MSL 2, 235°C
 JEDEC MS-012-16

Figure 8: 16L SOIC Mechanical Outline

16L 300mil CSOP

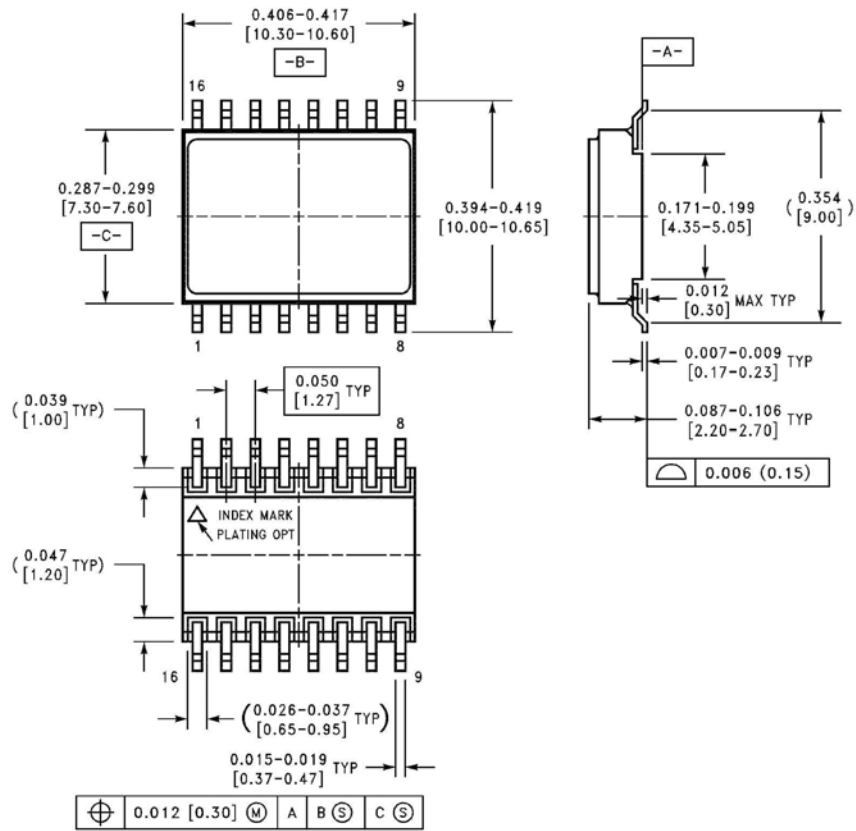


Figure 9: 16L CSOP Mechanical Outline

Table 6: Ordering Information

DEI Part Number	Marking	Package	OP. Temp. Range	Processing
DEI1054	DEI1054	16 lead NB SOIC	-55 / +85 °C	Standard
DEI1054-WMS	DEI1054-WMS	16 lead ceramic SOP	-55 / +125°C	Standard
DEI1054-WMB	DEI1054-WMB	16 lead ceramic SOP	-55 / +125°C	Burn-In, 96 hr @ 125°C

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