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DEI1041

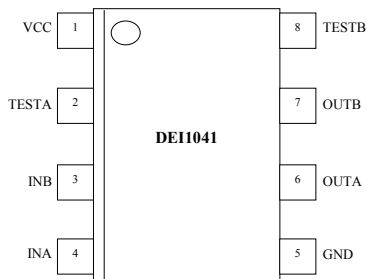
ARINC 429 LINE RECEIVER

FEATURES

- ARINC 429 to TTL/CMOS logic line receiver
- Operates from single +5V \pm 10% or 3.3V \pm 10% power supply
- ARINC inputs internally protected to lightning requirements of DO-160D Level A3
- Operates in high noise environment
 - Input Common Voltage Range: \pm 20V
 - 2V minimum Input hysteresis
- Logic level TEST inputs bypass analog inputs.
- 8 Lead SOIC.
- Replacement for HI-8588 and HI-8588-10

TERMINAL DESCRIPTION

Table 1 Terminal Description



NAME	DESCRIPTION
INA	429 INPUT. ARINC 429 format serial digital data "A" input.
INB	429 INPUT. ARINC 429 format serial digital data "B" input.
TESTA	LOGIC INPUT. Test input A.
TESTB	LOGIC INPUT. Test input B.
OUTA	LOGIC OUTPUT. CMOS/TTL format serial digital data "A" output.
OUTB	LOGIC OUTPUT. CMOS/TTL format serial digital data "B" output.
VDD	POWER INPUT. 5 VDC OR 3.3VDC.
GND	POWER INPUT. Ground.

FUNCTIONAL DESCRIPTION

The DEI1041 is a BICMOS device which contains one ARINC 429 differential line receiver. It translates incoming ARINC 429 data bus signals (tri-level RZ bipolar differential modulation) to a pair of TTL/CMOS logic outputs. It meets the requirements of the ARINC 429 Digital Information Transfer Standard. Refer to Figure 1 “DEI1041 Block Diagram and Truth Table”.

The device is designed to operate in a high noise environment. Inputs are accepted over a +/- 20V common mode voltage range and the receivers provide over 2 Volts of hysteresis. Circuit speed is optimized to reject high frequency transients.

All ARINC input pins are designed with internal protection from damage due to transients meeting the lightning induced transient requirements of DO-160D Level A3. The ARINC inputs may optionally be connected to ARINC bus through external 10k ohm series resistors. These resistors may be added in combination with transient voltage suppressors to achieve lightning protection beyond the Level A3 limits due to high input impedance.

The DEI1041 device provides logic level TEST inputs for built in system test. They force the receiver outputs to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the device is in test mode.

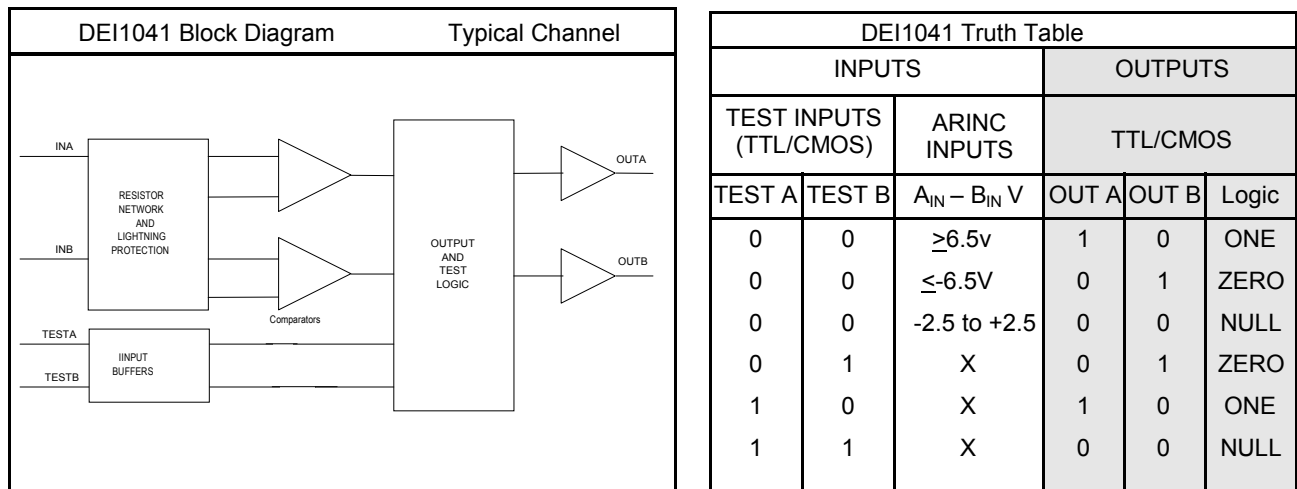


Figure 1 DEI1041 Block Diagram and Truth Table

ELECTRICAL DESCRIPTION

Table 2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	Vdd	+5V ± 10% +3.3V ± 10%
Logic Input Levels	VTESTA,B	0 to Vdd
Operating Temperature	Ta	-55 to +85°C -55 to +125°C
-SES		
-SMS		

Table 3 Absolute Maximum Rating

PARAMETER	MIN	MAX	UNITS
Supply Voltage (with respect to V _{SS})	-0.3	7.0	V
Storage Temperature	-65	+150	°C
Input Voltage, continuous (ARINC Inputs)	-40	+40	V
Input Voltage (Test Inputs)	V _{SS} - 0.3	V _{DD} +0.3	V
Power Dissipation @ 85 °C		500	mW
Junction Temperature: T _{jmax} , (limited by molding compound T _g)		145	°C
Peak Body Temperature (IPC/JEDEC J-STD-20)		235	°C
Lightning Protection (ARINC 429 Channel Inputs and TESTA/TESTB Inputs) Waveform 3* Waveform 4 and 5*	-600 -300	+600 +300	V V
*Per DO160D level 3A. See Figures 4-6.			
ESD per JEDEC A114-A Human Body Model		2000	V
Stresses above these limits can cause permanent damage.			

Table 4 Electrical Characteristics

Conditions: Temperature: -55°C to +85°C (SES) : -55°C to +125°C (SMS); V _{DD} = +5V ± 10% or 3.3V ± 10%						
PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
ARINC INPUTS						
V _A - V _B = Logic +1	OUTA = 1	V ₊₁	6.5	10	13	V
V _A - V _B = Logic -1	OUTB = 1	V ₋₁	-6.5	-10	-13	V
V _A - V _B = Logic Null	OUTA = 0 OUTB = 0	V _{NULL}	-2.5	0	2.5	V
Input Hysteresis		V _{HY}	2.0		4.0	V
V _A - V _B = Null to +1 transition	OUTA = 0→1	V _{T+1+}	5.5		6.5	V
V _A - V _B = +1 to Null transition	OUTA = 1→0	V _{T+1-}	2.5		3.5	V
V _A - V _B = Null to -1 transition	OUTB = 0→1	V _{T-1+}	-6.5		-5.5	V
V _A - V _B = -1 to Null transition	OUTB = 1→0	V _{T-1-}	-3.5		-2.5	V
Input Common Mode Voltage Range	Logic +1, Null, Logic -1	V _{CM}	-20		+20	V
Input Resistance IN _A to IN _B	V _{DD} open, Shorted to V _{SS} or +5V	R _{IN}	140k	390K		Ω
Input Resistance IN _A or IN _B to V _{SS}	V _{DD} open, Shorted to V _{SS} or +5V	R _S	140k	390K		Ω
Input Capacitance IN _A to IN _B	V _{DD} open, Shorted to V _{SS} or +5V (1)	C _{IN}			10	pF
Input Capacitance IN _A or IN _B to V _{SS}	V _{DD} open, Shorted to V _{SS} or +5V (1)	C _S			10	pF

Conditions: Temperature: -55°C to +85°C (SES) : -55°C to +125°C (SMS); V _{DD} = +5V ± 10% or 3.3V ± 10%						
PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
TEST INPUTS						
Logic 0 Voltage		V _{IL}			0.8	V
Logic 1 Voltage		V _{IH}	2.0			V
Logic 0 Current	V _{IL} = 0.8	I _{IL}			20	μA
Logic 1 Current	V _{IH} = 2.0	I _{IH}			20	μA
LOGIC OUTPUTS						
OUT A or OUT B	I _{OH} = 5mA (5V V _{dd}) I _{OH} = 1.5mA (3.3V V _{dd}) TTL Compatible	V _{OH}	2.4			V
OUT A or OUT B	I _{OL} = 5mA (5V V _{dd})	V _{OL}			0.5	V
	I _{OL} = 1.5mA (3.3V V _{dd})				0.4	
	TTL Compatible					
OUT A or OUT B	I _{OH} = 100μA CMOS Compatible	V _{OH}	V _{DD} - 50mV			V
OUT A or OUT B	I _{OL} = 100μA CMOS Compatible	V _{OH}			V _{SS} + 50mV	V
SUPPLY CURRENT						
V _{DD} Current	Data Rate = 0MHz, A/BIN =open, A/BOUT=open, V _{dd} = 5.5V or 3.63V	I _{DD}		2.5	5	mA

Notes:

1. Guaranteed by design, not production tested.
2. Current flowing into device is positive. Current flowing out of device is negative. All voltages are with respect to Ground unless otherwise noted.

Table 5 Switching Characteristics

PARAMETER	TEST CONDITION	SYMBOL	MAX	MAX	UNITS
			V _{dd} 3.3V	V _{dd} 5V	
INA/B to OUT A/B Prop Delay	TESTA = TESTB = 0 C _L = 50pF	t _{LH}	1000	900	nS
INA/B to OUT A/B Prop Delay	TESTA = TESTB = 0 C _L = 50pF	t _{HL}	1000	900	nS
Matching of t _{LH} and t _{HL}		Dtp	500	500	nS
OUT A/B rise time	10% to 90%, C _L = 50pF	t _r	50	25	nS
OUT A/B fall time	10% to 90%, C _L = 50pF	t _f	50	25	nS
TESTA/B to OUTA/B Prop delay	C _L = 50pF	t _{TOH}	100	60	nS
TESTA/B to OUTA/B Prop delay	C _L = 50pF	t _{TOL}	100	60	nS

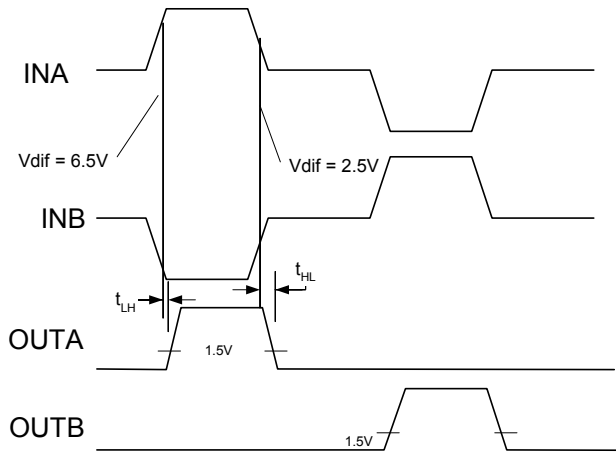


Figure 2 ARINC 429 Input to Logic Output Switching Waveform

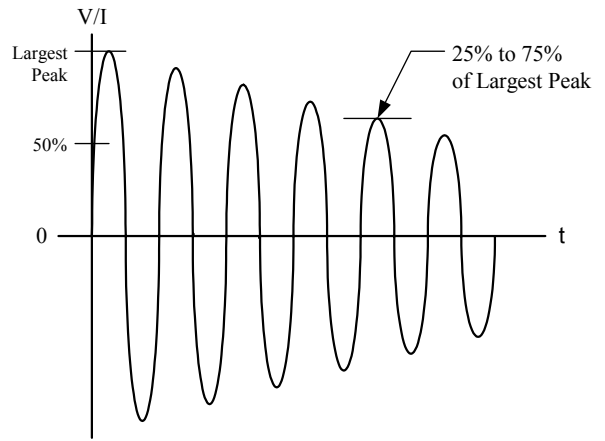


Figure 4 DO160D Lightning Induced Transient Voltage Waveform #3.
 Voc = 600V, Isc = 24A, Frequency = 1MHz \pm 20%

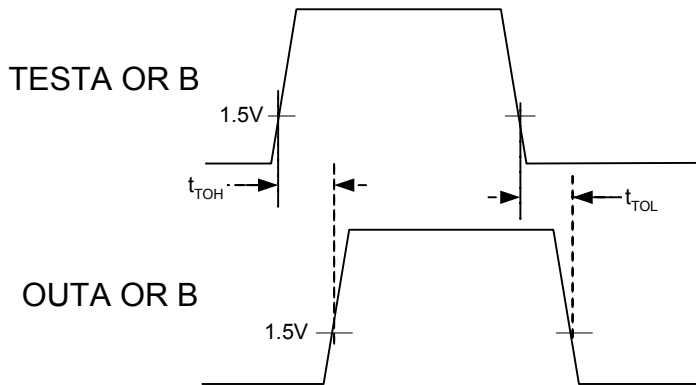


Figure 3 TEST Input to Logic Output Switching Waveform

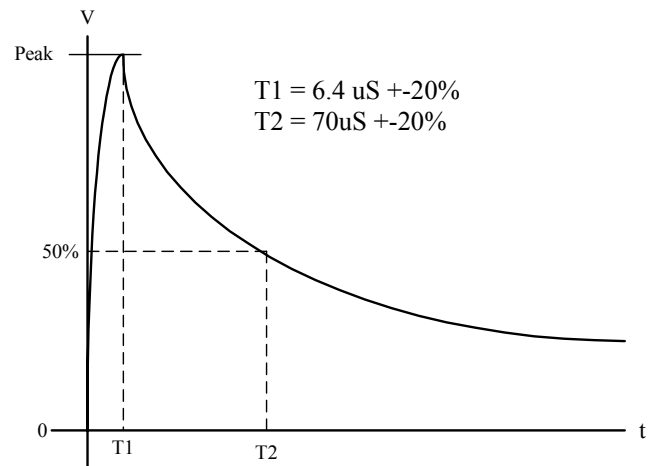


Figure 5 DO160D Lightning Induced Transient Voltage Waveform #4.
 Voc = 300V, Isc = 60A

LIGHTNING TRANSIENT NOTES:

1. Voc = Peak Open Circuit Voltage available at the calibration point.
2. Isc = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%.
4. The ratio of Voc to Isc is the generator source impedance to be used for generating the waveforms.

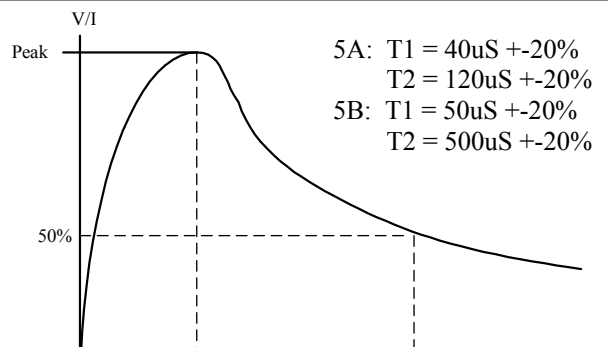


Figure 6 DO160D Lightning Induced Transient Voltage Waveform #5.
 Voc = 300V, Isc = 300A

PACKAGE DESCRIPTION

8 Lead SOIC

Table 6 8 Lead SOIC Characteristics

SYMBOL	DESCRIPTION	VALUE	UNITS
Theta _{jc}	Junction to Case	45	°C/W
Theta _{ja}	Junction to Ambient. 4 layer board with 2 internal power planes.	122	°C/W
MSL	JEDEC Moisture Sensitivity Level, 235°C	1	-

Dimension are in inches

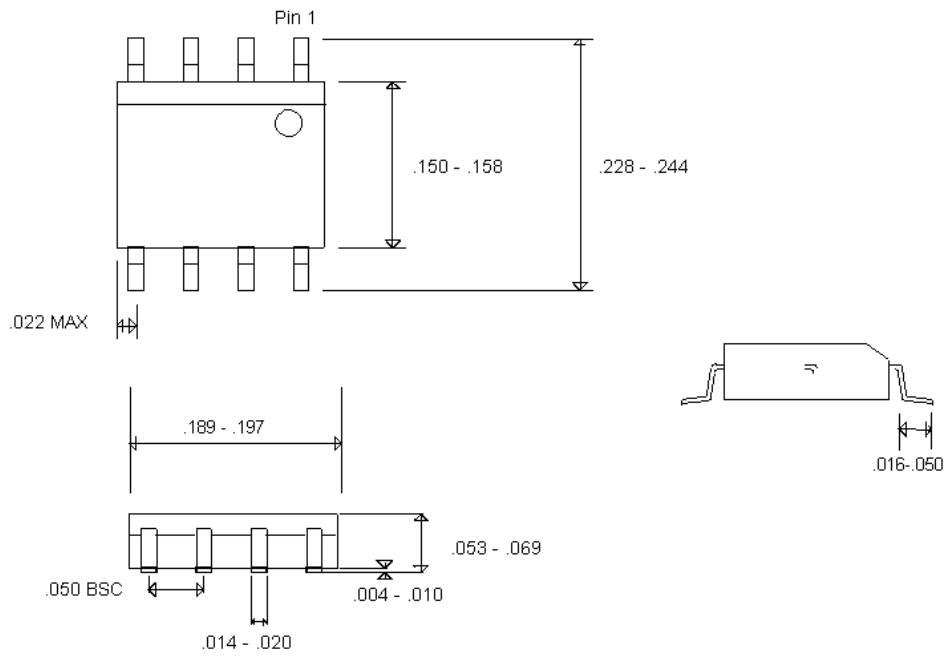


Figure 7 8L SOIC Mechanical Outline

PROCESS FLOW

Table 7 Process Flow

PROCESS STEP	PLASTIC STANDARD	PLASTIC BURN-IN
PRE-BURN-IN Electrical Test	N/A	YES
BURN IN (1)	N/A	96hrs @ +125 °C
FINAL ELECTRICAL TEST, Room Temperature	100%	100%
FINAL ELECTRICAL TEST, High Temperature	100% @ +85 or +125°C	100% @ +85 or +125°C
FINAL ELECTRICAL TEST, Low Temperature	0.65% AQL @ -55°C	0.65% AQL @ -55°C

NOTES:

1. Burn-in conditions: 125°C, 96 hrs, Vcc = 5.0V Inputs = 0V, Outputs open.

ORDERING INFORMATION

Table 8 Ordering Information

DEI PN	PART MARKING	TEMPERATURE RANGE	BURN-IN (1)	PACKAGE TYPE (1)
DEI1041-SES	DEI1041	-55/+85 °C	NO	8 lead SOIC
DEI1041-SMS	DEI1041M	-55/+125 °C	NO	8 lead SOIC
DEI1041-SMB	DEI1041B	-55/+125 °C	YES	8 lead SOIC

NOTES:

1. Contact factory for additional package options.

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