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**DEI1022, DEI1023
DEI1024, DEI1025
ARINC 429 Line Driver
Integrated Circuit**

Features:

- ARINC 429 Line Driver for high speed (100KHz) and low speed (12.5KHz) data rates.
- Adjustable Slew rates via external capacitors.
- Small foot print (14L SOIC NB)
- Programmable output differential range via V_{REF} pin.
- Drives full ARINC load of 400Ω and $0.03\mu F$.
- $-55^{\circ}C$ to $+85^{\circ}C$ operating temperature range.
- 100% Final testing.



Functional Description:

The ARINC 429 Line Driver Circuit is a bipolar monolithic IC designed to meet the requirements of several general aviation serial data bus standards. These include the differential bipolar RZ types such as ARINC 429, ARINC 571, and ARINC 575.

The DEI1022, DEI1023, DEI1024, and DEI1025 are a family of ARINC Line Driver circuits with variations in driver output resistance and output fusing. See the Product Matrix definition table below to find the correct version for your application.

Serial data is presented on DATA(A) and DATA(B) logic inputs in the dual rail format of the DEI1016. The driver is enabled by the SYNC and CLOCK inputs. The output voltage level is programmed by the V_{REF} input and is normally tied to +5VDC along with V_1 to produce output levels of +5 volts, 0 volts, and -5 volts on each output for ± 10 volts differential outputs.

The driver output resistance of the DEI1022 and DEI1023 is $75\Omega \pm 20\%$ at room temperature; 37.5Ω on each output. The driver output resistance of the DEI1024 and the DEI1025 is zero. The output slew rate is controlled by external timing capacitors on C_A and C_B . Typical values are $75pF$ for 100KHz and $500pF$ for 12.5KHz data.

Table 1: Product Matrix		
Part Number	Output Fusing	Output Resistance (each output)
DEI 1022	NO	37.5Ω
DEI 1023	YES	37.5Ω
DEI 1024	NO	0Ω
DEI 1025	YES	0Ω

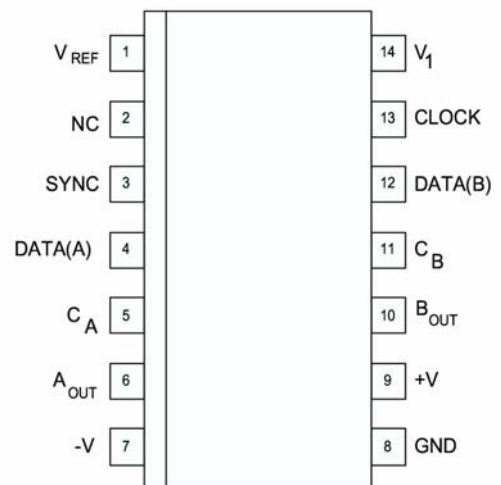


Figure 1: Pinout Diagram

Pin #	Pin Name	Table 2: Pin Descriptions
1	V _{REF}	Analog Input. The voltage on V _{REF} sets the output voltage levels on A _{OUT} and B _{OUT} . The output logic levels swing between +V _{REF} , 0 volts, and -V _{REF} volts.
2	NC	No Connect
3	SYNC	Logic input. Logic 0 forces outputs to NULL state. Logic 1 enables data transmission.
13	CLOCK	Logic input. Logic 0 forces outputs to NULL state. Logic 1 enables data transmission.
4 12	DATA(A) DATA(B)	Logic inputs. These signals contain the Serial Data to be transmitted on the ARINC 429 data bus. Refer to Figure 3.
5 11	C _A C _B	Analog Nodes. External timing capacitors are tied from these points to ground to establish the output signal slew rate. Typical C _A = C _B = 75pF for 100 kHz data and C _A = C _B = 500pF for 12.5 kHz data. *
6 10	A _{OUT} B _{OUT}	Outputs. These are the line driver outputs which are connected to the aircraft serial data bus.
7	-V	Negative Supply Input. -15VDC nominal.
8	GND	Ground.
9	+V	Positive Supply Input. +15VDC nominal.
14	V ₁	Logic Supply Input. +5VDC nominal.

*C_A and C_B pin voltages swing between ±5 volts. Any electronic switching of the capacitor on the pins must not inhibit the full voltage swings.

Table 3: Truth Table

INPUTS				OUTPUTS		COMMENTS
SYNC NOTE 1	CLOCK NOTE 1	DATA(A) NOTE 1	DATA(B) NOTE 1	A _{OUT}	B _{OUT}	
L	X	X	X	0	0	NULL
X	L	X	X	0	0	NULL
H	H	L	L	0	0	NULL
H	H	H	H	0	0	NULL
H	H	H	L	+V _{REF}	-V _{REF}	LOGIC 1
H	H	L	H	-V _{REF}	+V _{REF}	LOGIC 0

NOTES:

1. X = Don't Care

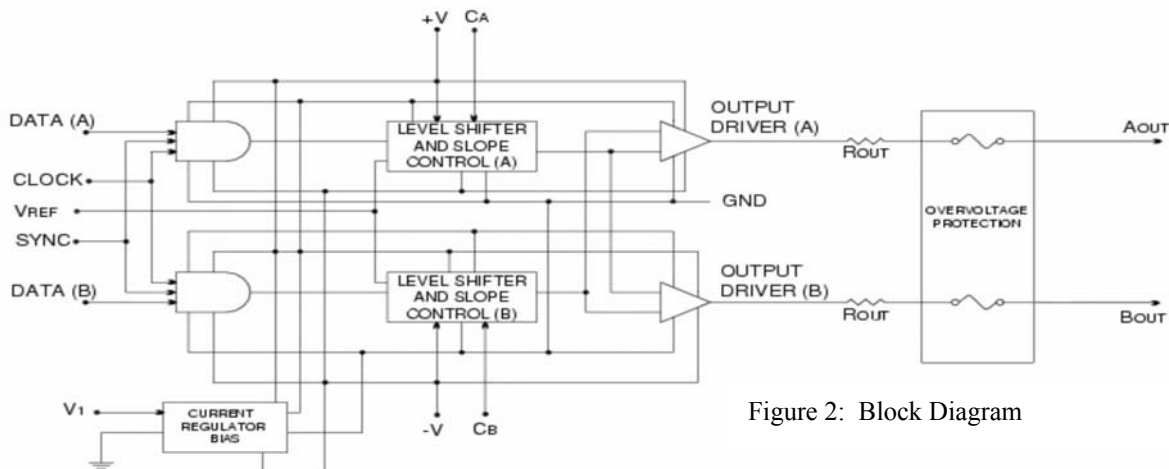


Figure 2: Block Diagram

Table 4: Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNITS
Voltage between pins +V and -V		40	V
V ₁ Maximum Voltage	V ₁	7	V
V _{REF} Maximum Voltage	V _{REF}	6	V
Logic Inputs		(GND-0.3V) to (V ₁ + 0.3V)	V
Lead Soldering Temperature (10 sec duration)	T _{SLD}	275	°C
Storage Temperature	T _{STG}	-65 to +150	°C
Max Junction Temperature Die Limit (short term operation)	T _{J MAX1}	+175	°C
Max Junction Temperature Plastic Package Limit (prolonged operation)	T _{J MAX2}	+145	°C
Output Short Circuit Duration	See Note 1		
Output Over-Voltage Protection	See Note 2		
Power Dissipation	See Table 6		

Notes:

- One output at a time can be shorted to ground indefinitely. Both outputs can be shorted indefinitely to ground or to each other for T_A < 45° C and Data Duty Cycle < 40%.
- Both DEI1023 and DEI1025 outputs are fused at between 0.5 Amp DC and 1.0 Amp DC to prevent an over-voltage fault from coupling onto the system power bus. The DEI1022 and DEI1024 outputs are not fused. External fusing must be provided to meet the Transmitter Fault Isolation of the ARINC 429 Specification.

Table 5: Operating Range

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Positive Supply Voltage	+V	+11.4		+16.5	VDC
Negative Supply Voltage	-V	-11.4		-16.5	VDC
V ₁	V ₁	+4.75	+5	+5.25	VDC
V _{REF} (For ARINC 429)	V _{REF}	+4.75	+5	+5.25	VDC
V _{REF} (For other applications)	V _{REF}	+3		+6	VDC
Operating Temperature	T _A	-55		+85	°C

Thermal Management

Device power dissipation varies greatly as a function of data rate, load capacitance, data duty cycle, and supply voltage. Proper thermal management is important in designs operating at the HI speed data rate (100KBS) with high capacitive loads and high data duty cycles.

Power dissipation may be estimated from Table 6 "Power Dissipation Table". Device power dissipation (Pd) is indicated for 100% data duty cycle with no word gap null times and should be adjusted for the appropriate data duty cycle (DC). Pd(application) = DC * [Pd(table) - 145mW] + 145mW, where DC is the application data duty cycle, Pd(table) is the Pd from the table for the indicated data rate and bus load, and 145mW is the quiescent power. The application's data duty cycle (DC) for 100KBS operation is calculated as:

$$DC = (\text{total bits transmitted in 10 sec period} / 1,000,000) = \\ (32 \times \text{total ARINC words transmitted in 10 sec period} / 1,000,000).$$

Heat transfer from the IC package should be maximized. Use maximum trace width on all power and signal connections at the IC. Place vias on the signal/power traces close to the IC to maximize heat flow to the internal power planes. If possible, design a solid heat spreader land under and beyond the IC to maximize heat flow from the device.

Table 6: Power Dissipation Table

100% Duty Cycle, Full Load = 400Ω/30,000pF Half Load = 4,000Ω/10,000pF

DATA RATE	LOAD	+V @ 15V	-V @ -15V	V ₁ , V _{REF} @ 5V	Pd POWER	LOAD POWER
0 to 100kbps	NONE	2.0mA	-5.0mA	4mA	125mW	0.0mW
12.5kbps	FULL	16.0mA	19.0mA	4mA	485mW	60.0mW
100kbps	FULL	48.0mA	51.0mA	4mA	1194mW *	325.0mW
12.5kbps	HALF	6.0mA	8.0mW	4mA	196mW	30.0mW
100kbps	HALF	22.0mA	25.0mA	4mA	561mW	162.5mW

* May require heat sink @ T_A = +85 °C**Table 7: DC Electrical Characteristics**Conditions: Temperature: -55°C to +85°C, +V = +11.4VDC to +16.5VDC, -V = -11.4VDC to -16.5VDC; V₁ = V_{REF} = +5VDC ±5%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I _{Q+V}	Quiescent +V supply current	-	2	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
I _{Q-V}	Quiescent -V supply current	-	5	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
I _{QV₁}	Quiescent V ₁ supply current	-	4	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
I _{QV_{REF}}	Quiescent V _{REF} supply current	-	10	-	μA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
V _{IH}	Logic 1 Input V	2.0	-	-	V	No Load.
V _{IL}	Logic 0 Input V	-	-	0.6	V	No Load.
I _{IH}	Logic 1 Input I	-	-	10	μA	No Load.
I _{IL}	Logic 0 Input I	-	-	-20	μA	No Load. (429/422' Pin I _{IL} = -2mA max)
I _{OHSC}	Output Short Circuit Current (Output High)	-80	-	-	mA	Short to Ground
I _{OLSC}	Output Short Circuit Current (Output Low)	80	-	-	mA	Short to Ground
V _{OH}	Output Voltage HIGH. (+1)	V _{REF} - 250mV	V _{REF}	V _{REF} + 250mV	V	No Load. 429 Mode.
V _{NULL}	Output Voltage NULL. (0)	-250	-	+250	mV	No Load. 429 Mode.
V _{OL}	Output Voltage LOW. (-1)	-V _{REF} - 250mV	-V _{REF}	-V _{REF} + 250mV	V	No Load. 429 Mode.
I _{CT} + -	Timing Capacitor Charge Current C _A (+1) C _B (-1) C _A (-1) C _B (+1)	-	+200 -200	-	μA μA	No Load. 429 Mode. SYNC = CLOCK = HIGH C _A and C _B held at zero volts.
ISC (+V)	+V Short Circuit Supply Current	-	-	+150	mA	Output short to ground
ISC (-V)	-V Short Circuit Supply Current	-	-	-150	mA	Output short to ground
R _{OUT}	Resistance on each output	-	SeeNotes	-	Ω	Room Temp Only
C _{IN}	Input Capacitor	-	-	15	pF	-

Notes: For DE11022 and DE11023, the typical resistance on each output is 37.5 Ω. For DE11024 and DE11025, the resistance on each output is 0 Ω.

AC ELECTRICAL CHARACTERISTICS

Figure 3 shows the output waveform for the ARINC 429.

The output slew rates are controlled by timing capacitors C_A and C_B . They are charged by $\pm 200\mu\text{A}$ (nom.). Slew rate (SR) measured as $\text{V}/\mu\text{sec}$, is calculated by:

$$\text{SR} = 200/C$$

where C is in pF.

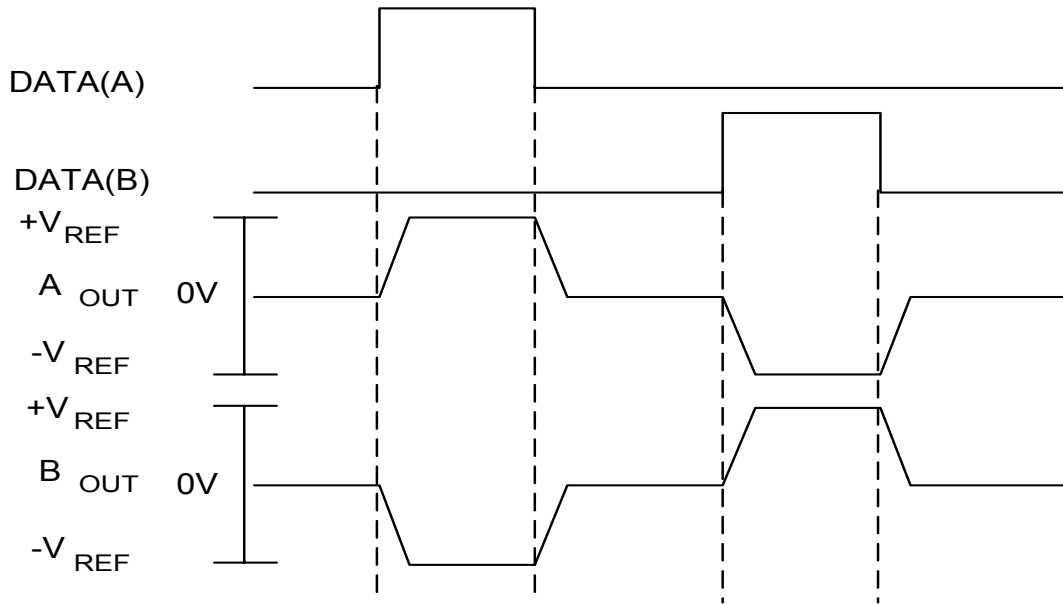


Figure 3: ARINC 429 Waveforms

Table 8: AC Electrical Characteristics

Parameter	Symbol	MIN	MAX	UNITS	NOTES
Output Rise Time A_{OUT} or B_{OUT} $C_A = C_B = 75\text{pF}$ $C_A = C_B = 500\text{pF}$	t_R t_R	1.0 5.0	2.0 15.0	μsec μsec	
Output Fall Time A_{OUT} or B_{OUT} $C_A = C_B = 75\text{pF}$ $C_A = C_B = 500\text{pF}$	t_F t_F	1.0 5.0	2.0 15.0	μsec μsec	
Input to Output Propagation Delay	t_{PNH} t_{PNL}	-	3.0	μsec	See Figure 4
A_{OUT} / B_{OUT} Skew Spec.	-	-	500	nsec	

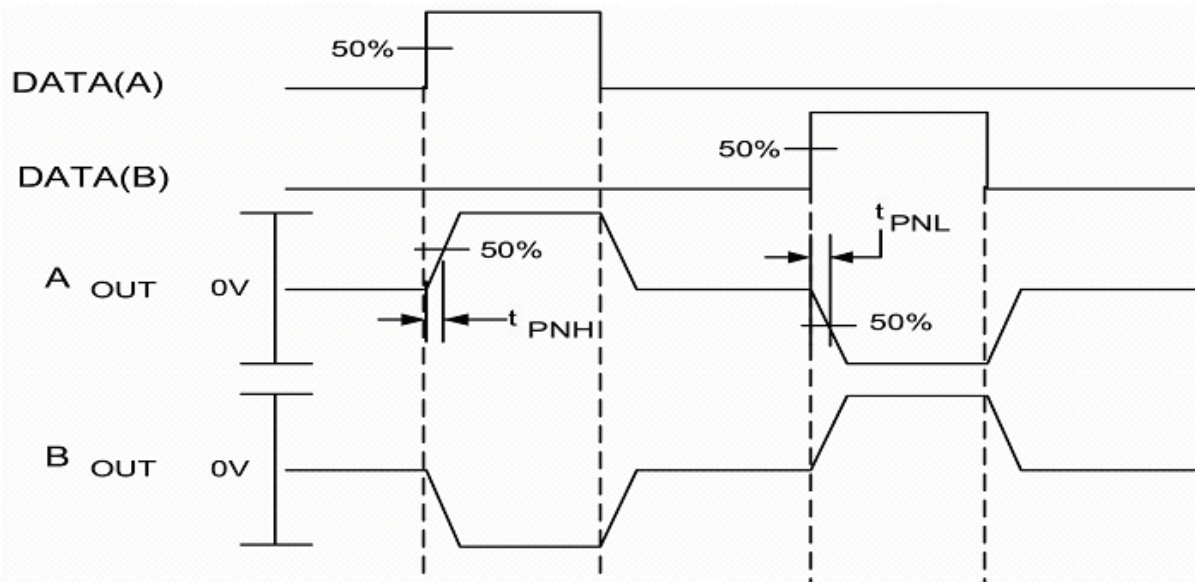
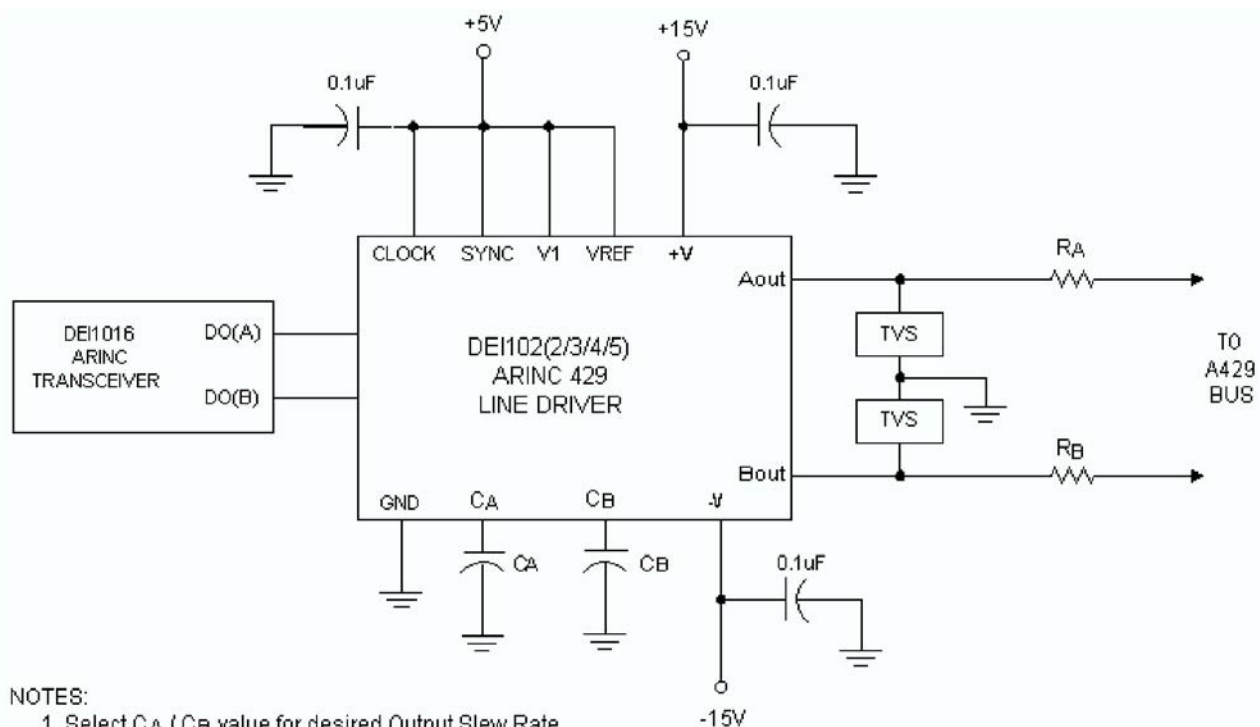


Figure 4: Propagation Delay



NOTES:

1. Select C_A / C_B value for desired Output Slew Rate.
2. TVS: TRANSIENT VOLTAGE SUPPRESSOR.
3. R_A / R_B : Use 37 Ohm for DE1102(4/5). Use Zero Ohm for DE1102(2/3).

Figure 5: Typical Application

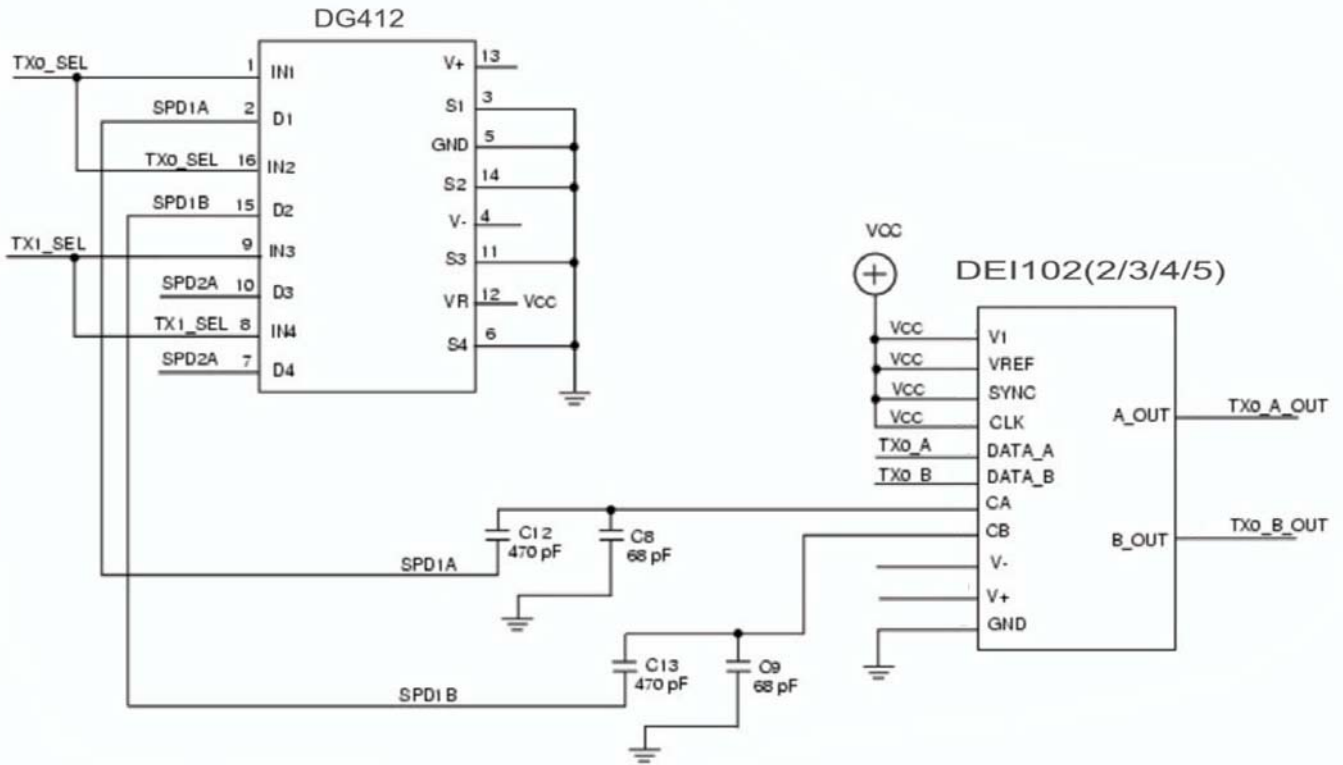


Figure 6: Typical Circuitry- Switching Capacitors For High-Speed/Low-Speed Operation

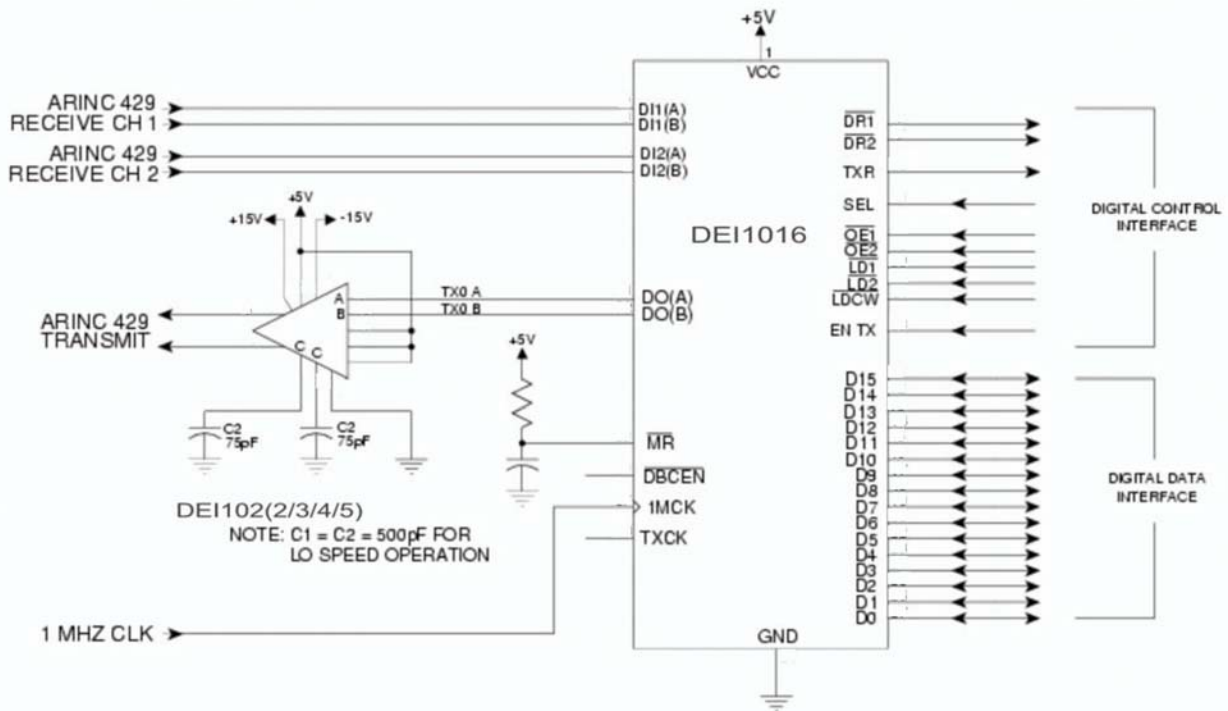


Figure 7: Typical Transceiver/Line Driver Interconnect Configuration

PACKAGE TYPE	14 Lead SOIC Narrow Body	14 Lead SOIC Narrow Body, Green
REFERENCE	14L SOIC NB G	14L SOIC NB G
THERMAL RESISTANCE:		
θ_{JA} (2 layer PCB)	115 °C/W	115 °C/W
θ_{JA} (4 layer PCB with Power Planes)	88 °C/W	88 °C/W
θ_{JC}	37 °C/W	37 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL (MSL)	MSL 2 / 235°C	MSL 2 / 260°C
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	SnPb	NiPdAu e4
Pb-Free DESIGNATION	Not Pb-free	RoHS Compliant
JEDEC REFERENCE	MS-012-AB	MS-012-AB

SCREENING	METHODS
ELECTRICAL TEST:	
ROOM TEMPERATURE	100%
HIGH TEMPERATURE	100% @ +125 °C
LOW TEMPERATURE	0.65% AQL@-55°C

DEI PART NUMBER	MARKING (1)	PACKAGE	TEMPERATURE RANGE	OUTPUT RESISTOR	OUTPUT FUSE
DEI1022	DEI1022	14 SOIC NB	-55 / +85 °C	37.5 Ω	NO
DEI1022-G	DEI1022 E4	14 SOIC NB G	-55 / +85 °C	37.5 Ω	NO
DEI1023	DEI1023	14 SOIC NB	-55 / +85 °C	37.5 Ω	YES
DEI1023-G	DEI1023 E4	14 SOIC NB G	-55 / +85 °C	37.5 Ω	YES
DEI1024	DEI1024	14 SOIC NB	-55 / +85 °C	0 Ω	NO
DEI1024-G	DEI1024 E4	14 SOIC NB G	-55 / +85 °C	0 Ω	NO
DEI1025	DEI1025	14 SOIC NB	-55 / +85 °C	0 Ω	YES
DEI1025-G	DEI1025 E4	14 SOIC NB G	-55 / +85 °C	0 Ω	YES

Notes:
1. All packages marked with Lot Code and Date Code. "E4" after Date Code denotes Pb Free category.

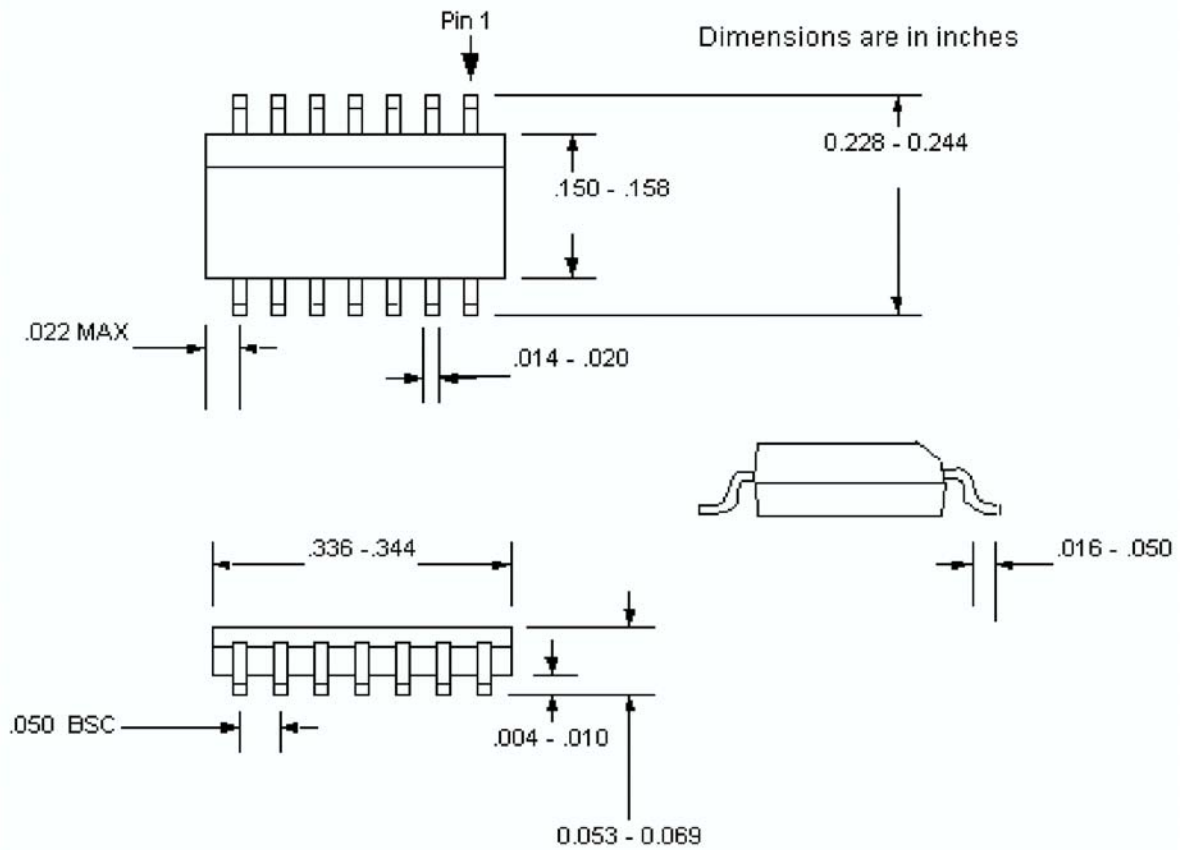


Figure 8: Package Dimensions (14L SOIC NB)

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