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# DEI 1028 Voltage Clamping Circuit

## Features

- Protection for power electronics on 28VDC avionics or industrial power bus.
- Controls power P-FET to clamp transient at 34V.
- Small foot print (8L SOIC NB).
- Wide input voltage range.
- Programmable Undervoltage Lockout.
- Logic compatible On/Off input.
- Stable over temperature.
- Soft start delay.



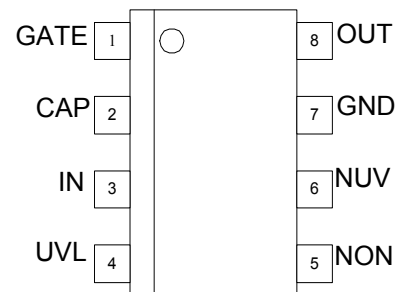
## General Description

The DEI1028 is a control circuit for a 28VDC power bus voltage clamp. It is designed for use as the front end to a 28VDC input power supply to provide transient voltage protection. It controls the gate drive of a P-Channel power MOSFET to linearly clamp the output during over voltage transients. The output voltage is maintained below the clamping threshold of 35V (max) which is adequate to protect most Commercial-Off-The-Shelf switching supplies, linear regulators, and op amps. The device protects against a 100V spike of 100ms duration and provides overshoot protection.

There is an Undervoltage Lockout feature that shuts the Power MOSFET off when the input voltage is below a user programmed threshold. An open collector logic output annunciates the under voltage status. There is also a logic on/off input which may be used to control the power circuit. An external capacitor may be used to set a delay from when input power is applied to when the MOSFET is turned on.

**Table 1: Pin Definitions**

Pin #	Name	Type / Description
1	<b>GATE</b>	<b>OUTPUT.</b> Controls the gate of the external p-channel power MOSFET.
2	<b>CAP</b>	<b>IN/OUT.</b> Controls the soft start delay of the device. Use 0.22uF for 200ms minimum soft start time.
3	<b>IN</b>	<b>INPUT.</b> Power input for the DEI1028 Voltage Clamp.
4	<b>UVL</b>	<b>INPUT.</b> Controls the under voltage lockout condition of the device.
5	<b>NON</b>	<b>INPUT.</b> Logic low enables device. Logic high disables device.
6	<b>NUV</b>	<b>OUTPUT.</b> Open collector output. Active low when IN is below UVL threshold.
7	<b>GND</b>	<b>POWER.</b> Ground
8	<b>OUT</b>	<b>INPUT.</b> Feedback to gate control from drain of Power MOSFET.



DEI1028 Pin Diagram

**Table 2: Absolute Maximum Ratings**

Parameter	Symbol	Rating	Units
IN Pin: Relative to GND Continuous 1 mS Transient 100 mS Transient	$V_{IN}$	0 to +40 -50 +100	V V V
UVL Pin: Relative to $V_{IN}$	$V_{UVL}$	-6 to +0.5	V
CAP Pin: Relative to $V_{IN}$	$V_{CAP}$	-20 to +20	V
GATE Pin: Relative to $V_{IN}$	$V_{GATE}$	-10 to +0.5	V
NON Pin: Relative to GND	$V_{NON}$	-0.5 to + 6.0	V
NUV Pin: Relative to GND	$V_{NUV}$	-0.5 to + 20	V
OUT Pin: Relative to GND	$V_{OUT}$	-0.5 to + 40	V
Operating Temperature	$T_A$	-55 to +85	°C
Storage Temperature	$T_{STG}$	-55 to +125	°C
Lead soldering temperature (10 sec duration)		+280	°C

**Table 3: Operating Characteristics — ( $T_a = -55\text{ °C}$  to  $85\text{ °C}$ )**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Clamp output voltage	$V_{O(CL1)}$	$V_{IN} = 40\text{ V}, 60\text{ V}$	33		35	V
Clamp output voltage	$V_{O(CL2)}$	$V_{IN} = 100\text{ V}^{(1)}$	33		35	V
Clamp output voltage	$V_{O(CL3)}$	$V_{IN} = -50\text{ V}^{(1,2)}$	-	-	-	
Source-Gate FET voltage (ON)	$V_{SG(1)}$	$R_{UVL} = 13.6\text{ k}\Omega, V_{IN} = 14\text{ V}$	9		10	V
Source-Gate FET voltage (OFF)	$V_{SG(2)}$	$R_{UVL} = 13.6\text{ k}\Omega, V_{IN} = 10\text{ V}$	0		0.7	V
Source-Gate FET voltage (ON)	$V_{SG(1)}$	$R_{UVL} = 7\text{ k}\Omega, V_{IN} = 25\text{ V}$	9		10	V
Source-Gate FET voltage (OFF)	$V_{SG(2)}$	$R_{UVL} = 7\text{ k}\Omega, V_{IN} = 19.5\text{ V}$	0		0.7	V
Source-Gate FET voltage (LINEAR)	$V_{SG(3)}$	$35\text{ V} < V_{IN} < 100\text{ V},$ $V_{OUT} = \text{Clamp Voltage (33—35v)}$	0.7		9	V
Turn-on time	$t_{ON}$	$C = 0.22\mu\text{F}$ ; see Figures 4, 5.	200			msec
Soft start delay charge current	$I_{ST}$	$V_{IN} > 10\text{ V}$	0.75		3	$\mu\text{A}$
Soft start delay threshold	$V_{ST}$	$V_{IN} > 10\text{ V}$	$V_{IN} - 2.5$		$V_{IN} - 2.9$	V
Output overshoot voltage	$V_{OMX}$	See Figure 6. <sup>(1)</sup>			35	V
Output settling time	$t_S$	See Figure 6. <sup>(1)</sup>			2	msec
Supply Current	$I_{IN}$	$V_{IN} = 30\text{ V}$			5	mA

## Notes:

- Guaranteed by design and not production tested.
- Device must survive this test. Duration of negative voltage must be limited to less than 1 ms due to heating effects.
- MOSFET capacitance ( $C_{gs}$ ) must be in the range 500 ~ 5000 pF. If below 500 pF, an external 470 pF capacitor must be connected between the DEI1028 OUT and GATE pins.

**Table 4: Logic Characteristics — ( $T_a = -55\text{ °C}$  to  $85\text{ °C}$ )**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
NON input logic 1 level	$V_{IH}$	$V_{IN} = 8\text{ to }30\text{ V}$	2.8			V
NON input logic 0 level	$V_{IL}$	$V_{IN} = 8\text{ to }30\text{ V}$			0.8	V
NON input logic 0 current	$I_{IL}$	$V_{NON} = 0\text{ V}$ $V_{IN} = 8\text{ to }30\text{ V}$	-300		-30	$\mu\text{A}$
NUV output logic 1 level	$V_{OH}$	$R_{UVL} = 13.6\text{ k}\Omega, V_{IN} = 14\text{ V},$ $R_{PU} = 10\text{ k}\Omega\text{ to }5\text{ V}$ (See Figure 7.)	4.75			V
NUV output logic 0 level	$V_{OL}$	$R_{UVL} = 13.6\text{ k}\Omega, V_{IN} = 10\text{ V}$ $I_{OL} = 420\text{ }\mu\text{A}$ (See Figure 7.)			0.8	V

## Gate Drive

The DEI1028 device is designed to control the gate of a P-Channel power MOSFET such as the IRF9540. At normal operation the gate output turns the transistor ON to saturation. Below under voltage conditions the MOSFET is shut off. In clamp mode the MOSFET is driven to linear mode, keeping the output at approximately 34 V.

## Undervoltage Lockout

An Undervoltage Lockout feature is provided to prevent large currents from flowing through the MOSFET if the input voltage is too low. The resistor is placed between the IN and UVL pins. The following formula is used to determine the resistor value to set the nominal (25 °C) lockout threshold voltage: (see figures 6 & 7 for temperature characteristics)

$$R_{UVL} = (100k\Omega) \frac{1.45}{(V_{UVL} - 1.45)}$$

## Soft Start Delay

An external capacitor between CAP and the input voltage may be used to set a turn on delay time. See figure 4.

$$T_{ON}(mS) \approx C_{SS}(nF)$$

At start up, the voltage across the capacitor is approximately zero, the voltage at the CAP pin is approximately the input voltage, and the MOSFET is turned off. The 1028 CAP pin provides a current sink (approx. 2uA) to charge the capacitor. The 1028 turns the MOSFET on when the voltage across the capacitor reaches approximately 2.7V.

**Table 4: Under voltage Lockout Threshold**

$R_{UVL}$	TEMP	SYMBOL	MIN	TYP	MAX	UNITS
13.6K	85 °C	$V_{IN}$	12.0	-	14.0	V
13.6K	25 °C	$V_{IN}$	11.0	-	13.0	V
13.6K	-55 °C	$V_{IN}$	10.0	-	12.0	V
7K	85 °C	$V_{IN}$	22.0	-	24.0	V
7K	25 °C	$V_{IN}$	21.0	-	23.0	V
7K	-55 °C	$V_{IN}$	19.5	-	21.5	V

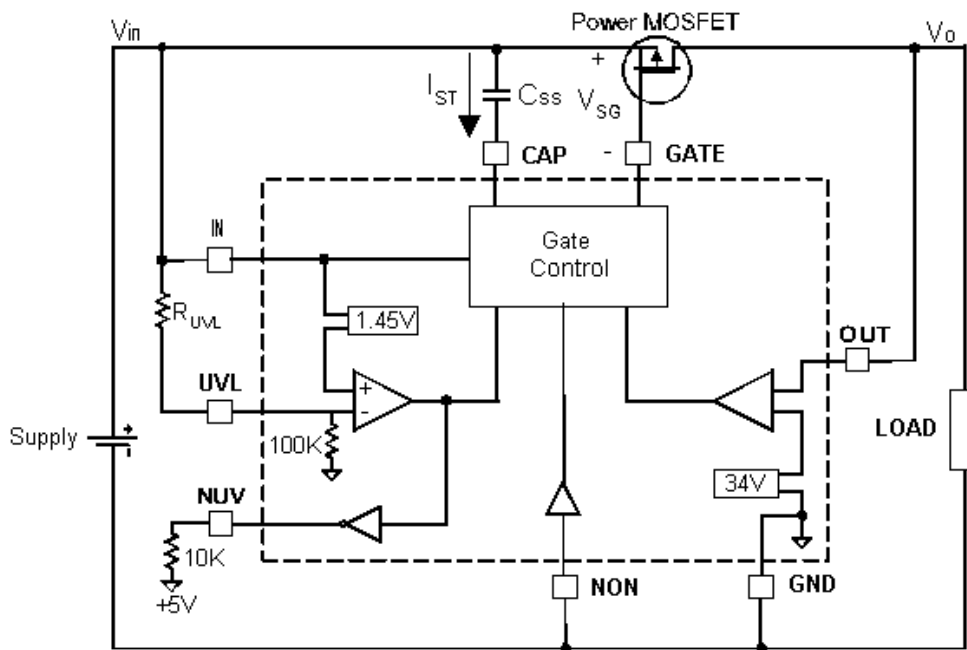


Figure 1: Typical Application

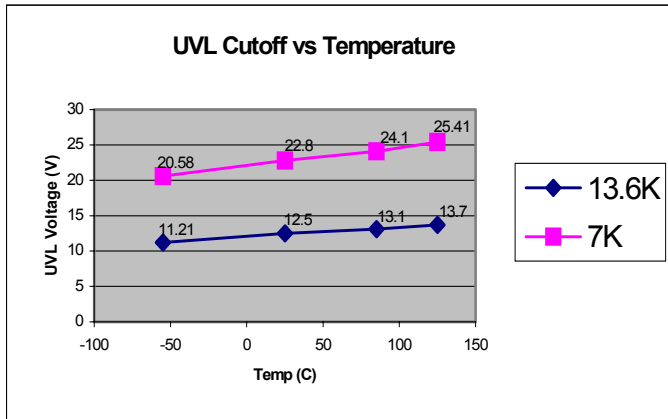


Figure 2:  
Typical UVL cutoff voltage by temperature for  $R_{UVL} = 7K$  and  $R_{UVL} = 13.6K$

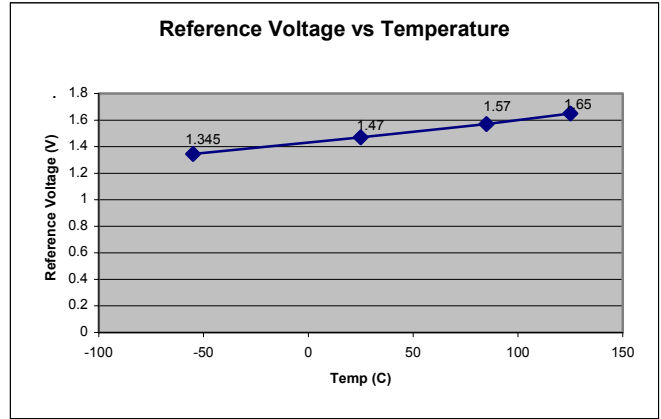


Figure 3:  
Typical UVL Reference Voltage vs. Temperature.

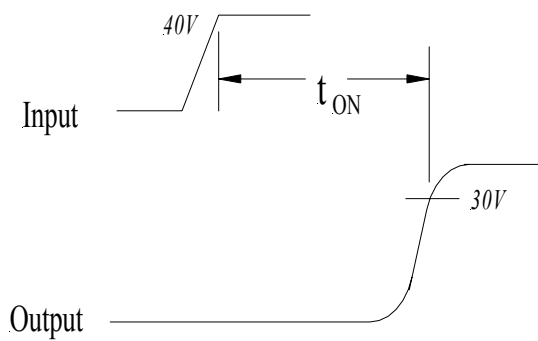


Figure 4. Turn On Time

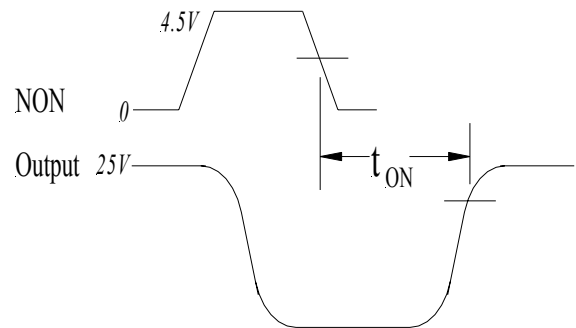


Figure 5. Logic Control ("NON" pin)

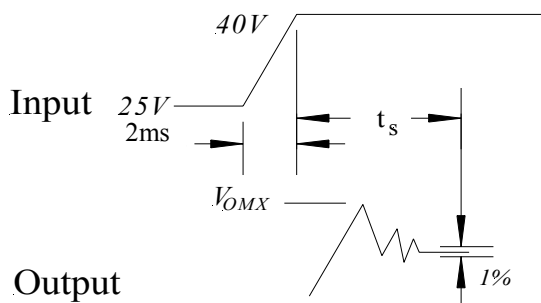


Figure 6. Overshoot and Settling

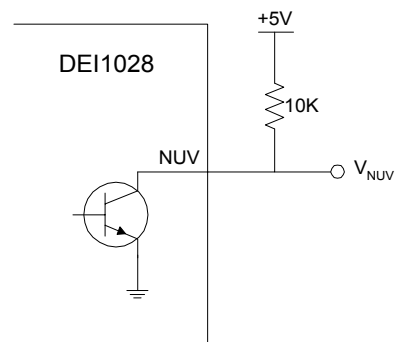


Figure 7. Undervoltage Logic Output

**Package Characteristics:**

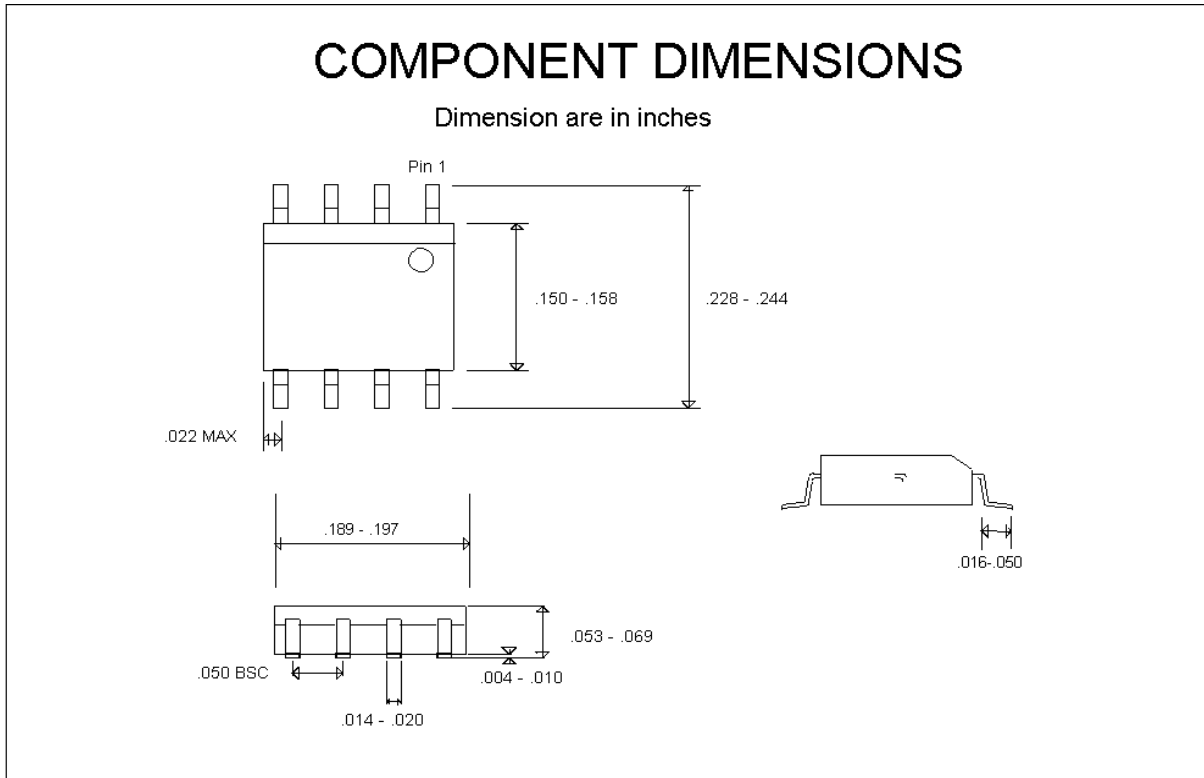


Figure 8: 8 Lead SOIC Outline Drawing

Moisture Sensitivity: JEDEC J-STD-020A MSL 1

Table 7: 8 LD SOIC — Thermal Characteristics			
Theta <sub>jc</sub>	Junction to Case	40	°C/W
Theta <sub>ja</sub>	Junction to Ambient 4 layer board	135	°C/W
T <sub>j-MAX</sub>	Max Junction Temperature	125	°C

Table 8: Ordering Information			
Part Number	Marking	Package	Temp
DEI1028-SES	DEI1028	8-lead SOIC	-55 / +85 °C

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